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| <b>INFORMATION DISCLOSURE</b><br><br><b>STATEMENT BY APPLICANT</b><br><br>(use as many sheets as necessary) |                        | Application Number   | 10/599,593   |
|   |                        | Filing Date          | 10-02-2006   |
|   |                        | Confirmation No.     | 1321         |
|   |                        | First Named Inventor | Dutt         |
|   |                        | Art Unit             | 2193         |
|   |                        | Examiner Name        | Wang, Jue S. |
| Sheet 1 of 1  | Attorney Docket Number | 703538.4054          |              |

| U.S. PATENT DOCUMENTS |                       |   |  |
|-----------------------|-----------------------|---|--|
| Examiner Initials     | Cite No. <sup>1</sup> | U.S. Patent Document Number-Kind Code <sup>2</sup> (if known) | Publication Date MM-DD-YYYY<br>Name of Patentee or Applicant of Cited Document |
|                       | AA                    |   |  |
|                       | AB                    |   |  |
|                       |                       |   |  |

| OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS |                       |   |                |
|---|-----------------------|---|----------------|
| Examiner Initials <sup>1</sup>                    | Cite No. <sup>1</sup> | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.   | T <sup>2</sup> |
|   | BA                    | FUTAMURA, Y., Partial Evaluation of Computation Process: an Approach to a Compiler-Compiler, Higher-Order and Symbolic Computation 12, 391-391. 1999 (updated and revised version of Partial Evaluation of Computation Process: an Approach to a Compiler-Compiler, Systems, Computers, Controls, Volume 2(5), 1971, pgs. 45-50). |                |
|   | BB                    | Nohl, A. et al., A Universal Technique for Fast and Flexible Instruction-Set Architecture Simulation, DAC 2002.   |                |
|   | BC                    | HALAMBI, A. et al., EXPRESSION: A Language for Architecture Exploration through Compiler-Simulator Retargetability, DATE 1999.  |                |
|   | BD                    | HARTOOG, M. et al. Generation of Software Tools from Processor Descriptions for Hardware/Software Codesign, DAC 1997  |                |
|   | BE                    | RESHADI, M. et al., Reducing Compilation Time Overhead in Compiled Simulators, ICCD 2003, October 13-15, 2003, pgs. 151-153.  |                |
|   | BF                    | RESHADI, M. et al., Instruction Set Compiled Simulation: A Technique for Fast and Flexible Instruction Set Simulation, DAC 2003, June 2-6, 2003, pgs. 758-763.  |                |
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|--------------------|------------|-----------------|------------|
| Examiner Signature | /Jue Wang/ | Date Considered | 10/08/2011 |
|--------------------|------------|-----------------|------------|

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